Universität Bremen - Computer Architecture

Coverage of OCL Operation Specifications and Invariants

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1. Motivation and example



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- 2. Coverage in the design flow



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- 3. Coverage at the Formal Specification Level



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- 4. Implementation: USE plugin



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- 5. Experimental evaluation



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- 6. Conclusion



Textual Specification



















Class diagram 💥				цк	d' X
Processor					
pc : Integer instruction : Integer	processor	Controller address : Integer	controller	Cell	
prepareMemory() fetch() process()	programMemory	write(content : Integer) read()		cells content : Integer	



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- Consistency
- Executability of operations

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- Executability of operations
- Reachability of a deadlock state

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Implementation level:

- Line coverage
- Statement coverage
- Branch/decision coverage
- Path coverage
- Loop coverage



Formal Specification Level:

 Different metrics for different diagrams/model types



Formal Specification Level:

- Different metrics for different diagrams/model types
- Fewer metrics



Formal Specification Level:

- Different metrics for different diagrams/model types
- Fewer metrics
- Code coverage at the FSL?



Coverage at the FSL

Input: UML class diagram m with OCL constraints, operation call sequences ${\cal S}$



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1. Operation call coverage: How many operations from m have been called in S?







 σ_0

 σ_1









Operation call coverage: 40%

Coverage at the FSL

- Input: UML class diagram m with OCL constraints, operation call sequences S
 - 1. **Operation call coverage:** How many operations from m have been called in S?
 - 2. Subexpression coverage: How many constraints from m have evaluated to true during the execution of S?



 σ_0

 σ_1

 σ_2



process itself has been executed



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- post24: pc@pre = 9 implies pc = 0



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Problem: constraints might never become true



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Problem: constraints might never become true \rightarrow dead code



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 - (b) For each subexpression se

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 - Recalculate subexpression coverage



Example: Processor::process()

post24: pc@pre = 9 implies pc = 0Uncovered subexpressions *se*: {pc@pre = 9, pc = 0}





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USE Plugin

Coverage	막다 🗵				
Initial Coverage Maximum Coverage					
read	Not Covered				
pre3: self.address.isDefined					
post8: self.cells->forAll(c : Cell ((c.address = c.address@pre) and (c.content = c.content@pre)))					
post9: self.cells->one(c : Cell ((c.address = self.address@pre) and (c.content = self.dataout)))	Not Covered				
post10: self.address.isUndefined					
post11: (self.processor.instruction = self.processor.instruction@pre)	Not Covered				
post12: (self.processor.pc = self.processor.pc@pre)	Not Covered				
write	Not Covered				
prel: (self.address < 10)	Not Covered				
pre2: (content < 4)	Not Covered				
post1: self.cells->one(c : Cell ((c.address = self.address) and (c.content = content)))	Not Covered				
post2: self.cells->forAll(c : Cell (c.address = c.address@pre))	Not Covered				
post3: self.cells->forAll(c : Cell ((c.address <> self.address) implies (c.content = c.content@pre)))	Not Covered				
post4: (self.processor.instruction = self.processor.instruction@pre)	Not Covered				
post5: (self.processor.pc = self.processor.pc@pre)	Not Covered				
post6: (self.dataout = self.dataout@pre)	Not Covered				
post7: (self.address = self.address@pre)	Not Covered				
fetch	Not Covered				
pre5: self.programMemory.dataout.isDefined	Not Covered				
post18: (self.instruction = self.programMemory.dataout@pre)	Not Covered				
post19: (self.pc = self.pc@pre)					
post20: self.programMemory.cells->forAll(c : Cell ((c.address = c.address@pre) and (c.content = c.content@pre)))					
post21: (self.programMemory.address = self.programMemory.address@pre)	Not Covered				
post22: self.programMemory.dataout.isUndefined	Not Covered				
prepareMemory	Not Covered				
pre4: self.programMemory.address.isUndefined	Not Covered				
post13: (self.programMemory.address = self.pc)	Not Covered				
post14: (self.instruction = self.instruction@pre)	Not Covered				
post15: (self.pc = self.pc@pre)	Not Covered				
post16: (self.programMemory.dataout = self.programMemory.dataout@pre)	Not Covered				
post17: self.programMemory.cells->forAll(c : Cell ((c.address = c.address@pre) and (c.content = c.content@pre)))	Not Covered				
process	Covered				
pre6: self.instruction.isDefined	Covered				
post23: ((self.pc@pre < 9) implies (self.pc = (self.pc@pre + 1)))	Maybe Covered				
post24: ((self.pc@pre = 9) implies (self.pc = 0))	Maybe Covered				
post25: self.programMemory.cells->forAll(c : Cell ((c.address = c.address@pre) and (c.content = c.content@pre)))	Covered				
post26: self.instruction.isUndefined	Covered				
post27: (self.programMemory.address = self.programMemory.address@pre)	Covered				
post28: (self.programMemory.dataout = self.programMemory.dataout@pre)	Covered				
Initial: Covered 6/39 Elements	15%				
Maximum: Covered 14/39 Elements	36%				

USE Plugin

Coverage	지 고 고			
Initial Coverage Maximum Coverage				
read	Not Covered			
pre3: self.address.isDefined	Not Covered			
post8: self.cells->forAll(c : Cell ((c.address = c.address@pre) and (c.content = c.content@pre)))	Not Covered			
post9: self.cells->one(c : Cell ((c.address = self.address@pre) and (c.content = self.dataout)))	Not Covered			
post10: self.address.isUndefined	Not Covered			
post11: (self.processor.instruction = self.processor.instruction@pre)	Not Covered			
post12: (self.processor.pc = self.processor.pc@pre)	Not Covered			
write	Not Covered			
prel: (self.address < 10)	Not Covered			
pre2: (content < 4)	Not Covered			
post1: self.cells->one(c : Cell ((c.address = self.address) and (c.content = content)))	Not Covered			
post2: self.cells->forAll(c : Cell (c.address = c.address@pre))	Not Covered			
post3: self.cells->forAll(c : Cell ((c.address <> self.address) implies (c.content = c.content@pre)))	Not Covered			
post4: (self.processor.instruction = self.processor.instruction@pre)	Not Covered			
post5: (self.processor.pc = self.processor.pc@pre)	Not Covered			
post6: (self.dataout = self.dataout@pre)	Not Covered			
post7: (self.address = self.address@pre)	Not Covered			
fetch	Covered			
pre5: self.programMemory.dataout.isDefined	Covered			
post18: (self.instruction = self.programMemory.dataout@pre)				
post19: (self.pc = self.pc@pre)				
post20: self.programMemory.cells->forAll(c : Cell ((c.address = c.address@pre) and (c.content = c.content@pre)))				
post21: (self.programMemory.address = self.programMemory.address@pre)				
post22: self.programMemory.dataout.isUndefined				
prepareMemory				
pre4: self.programMemory.address.isUndefined	Not Covered			
post13: (self.programMemory.address = self.pc)	Not Covered			
post14: (self.instruction = self.instruction@pre)	Not Covered			
post15: (self.pc = self.pc@pre)	Not Covered			
post16: (self.programMemory.dataout = self.programMemory.dataout@pre)	Not Covered			
post17: self.programMemory.cells->forAll(c : Cell ((c.address = c.address@pre) and (c.content = c.content@pre)))	Not Covered			
process	Covered			
pre6: self.instruction.isDefined	Covered			
post23: ((self.pc@pre < 9) implies (self.pc = (self.pc@pre + 1)))	Covered			
post24: ((self.pc@pre = 9) implies (self.pc = 0))	Partially Covered			
post25: self.programMemory.cells->forAll(c : Cell ((c.address = c.address@pre) and (c.content = c.content@pre)))	Covered			
post26: self.instruction.isUndefined	Covered			
post27: (self.programMemory.address = self.programMemory.address@pre)	Covered			
post28: (self.programMemory.dataout = self.programMemory.dataout@pre)	Covered			
Initial: Covered 6/39 Elements	15%			
Maximum: Covered 14/39 Elements	36%			



Experimental Evaluation

Model	Initial	Maximal	#Sequences	Run-time
CPU	0%	0%	0	<0.01s
Traffic	35%	94%	4	< 0.01 s
Memory	15%	97%	6	0.22s
Car	0%	100%	4	$<\!0.01s$
Life	0%	100%	3	< 0.01 s



Two new coverage metrics for the FSL



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- Detect dead code before the implementation



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- Generate operation call sequences which can be also used as test cases

- Two new coverage metrics for the FSL
- Detect dead code before the implementation
- Generate operation call sequences which can be also used as test cases
- Future work: more sophisticated metrics, in particular functional coverage

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